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10/649,906	08/26/2003	William Robert Haas	100201032-1	5761

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EXAMINER

GOLDEN, JAMES R

ART UNIT PAPER NUMBER

2187

DATE MAILED: 09/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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## Office Action Summary

Application No.

10/649,906

Applicant(s)

HAAS ET AL.

Examiner

James Golden

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 31 January 2005.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

The instant application having Application Number 10/649906 has a total of 12 claims pending; there are 4 independent and 8 dependent claims, all of which are ready for examination by the examiner.

#### ***Drawings***

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: 105 of line 309 of the Detailed Description.
2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference characters not mentioned in the description: 325, 330 of Fig. 3. These labels appear to refer to lines 249-250 of the Detailed Description.
3. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Specification***

4. The disclosure is objected to because of the following informalities:

in line 35, the phrase "often times" should be condensed to a single word, and the comma following it should be removed;

in line 82, "design" should be corrected to "designate";

in line 128, "bus" is referred to as 100 of Fig. 1, but 100 is not labeled as "controller" in the drawings, so this element number should be changed to 160, which is labeled "bus" in the drawings and which is used to refer to "bus" in line 147;

in line 172, "communications" should be changed to "communicates";

in line 309, the elements referred to by "two data paths and two power paths between the devices (100, 105)" should be corrected, as 105 is not shown in the drawings;

in line 333, "module" is misspelled in the phrase "the controller moduel 100," [sic];

the meaning of the sentence found on lines 334-339 is unclear, and the sentence should be broken up.

Appropriate correction is required.

***Claim Objections***

5. Claim 3 is objected to because of the following informalities: "to" is missing between "in response" and "empty data indication," lines 9-10.
6. Claims 8-10 are objected to because of the following informalities: "predetermined" is misspelled in lines 1-2 of claim 8. Claims 9 and 10 are objected to because they inherit this deficiency of claim 8. Appropriate correction is required.
7. Claim 10 is objected to under 37 CFR 1.75 as being a substantial duplicate of claim 9. See MPEP § 706.03(k).
8. Claim 11 is objected to because of the following informalities: "memory" from the phrase "first and second old memory having..." (lines 3-4) should be corrected to "memories" and the phrase "first and second old memories" (lines 4-5) should be removed.

***Claim Rejections - 35 USC § 102***

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Krech, Jr. et al. (US 5,664,114).
11. With respect to claim 1, Krech, Jr. et al. disclose a memory control system, comprising:  
  
a processor (110 of Fig. 1);

a bus in communication with the processor (input line to 102 of Fig. 1);  
a first memory ("memory" of 111 of Fig. 1) in communication with the processor  
in a first data path removed from the bus ("memory" of 111 of Fig. 1 on board 110;  
column 4, line 11 indicates that the memory is "on board" and therefore inherently  
removed from the bus); and

a second memory (112 of Fig. 1)  
in communication with the processor in a second data path removed from the  
bus (connection from microprocessor to memory 112) and  
having an empty memory indicator (column 5, lines 10-12);  
wherein, in response to the second memory containing no application data, the  
second memory provides a corresponding indication to the processor (column 5, lines  
10-12).

12. With respect to claim 2, Krech, Jr. et al. disclose a hub (105 of Fig. 1)  
in communication with the bus (connection between 102 and 105 of Fig. 1)  
to provide application data (column 3, line 67 – column 4, lines 1-2)  
to the processor (110 of Fig. 1).
13. With respect to claim 3, Krech, Jr. et al. disclose a memory control system,  
comprising:  
a controller module (110 of Fig. 1)  
having a first data path ("memory" of 111 of Fig. 1 on board 110; column 4, line  
11),  
a second data path (connection from microprocessor 110 to memory 112), and

a bus (input line to 102 of Fig. 1); and  
a first memory in communication with the first data path ("memory" of 111 of Fig. 1); and  
a second memory in communication with the second data path (112 of Fig. 1) and having an empty memory indicator (column 5, lines 10-12);  
wherein the controller module replicates data from the first memory to the second memory in response to an empty data indication from the second memory (column 6, lines 43-49).

14. With respect to claim 4, Krech, Jr. et al. disclose the system of claim 3, further comprising:

an application module (102 of Fig.1)  
in communication with (connection from 102 to 105 and 105 to 110)  
the controller module (110 of Fig.1),  
wherein the controller module is connected to retrieve application data from the application module for storage in the first memory (column 3, line 67 – column 4, lines 1-2).

15. With respect to claim 5, Krech, Jr. et al. disclose the system of claim 3, further comprising:

a memory module (composition of "memory" of 111 and 112 of Fig. 1)  
in communication with (111 on board 110, and connection from 110 to 112)  
the controller module (110 of Fig. 1)  
and containing the first memory ("memory" of 111 of Fig. 1)

and the second memory (112 of Fig. 1).

16. Claims 8-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Baentsch et al. (US 6,272,607).

17. With respect to claim 8, Baentsch et al. disclose a method of installing a new memory (9 of Fig. 1) that has a predetermined memory capacity into a system that comprises a processor (1 of Fig. 1) and first old memory (51 of Fig. 1), with the first old memory storing an amount of application data to produce a redundant array of independent memories, comprising:

initiating a duplication function in the processor (column 3, lines 9-15);

transmitting an empty data indication from the new memory to the processor (column 2, lines 61-67 – column 3, lines 1-2); and

replicating the application data from the first old memory to the new memory (column 3, lines 17-18 describe how the “data space” 5 of Fig. 1 of memory 9 of Fig. 1 is “filled with the object payload;” column 5, lines 57-58 describe how the payload data is “transmitted in segments from the RAM 51 to the EEPROM 50,” where the EEPROM contains memory block 9).

18. With respect to claims 9 and 10, Baentsch et al. disclose the method of claim 8, wherein replicating the application data comprises comparing the amount of application data in the first old memory to the capacity of the new memory to determine whether said capacity is sufficient to hold the application data (column 3, lines 11-12).

19. Claim 11 is rejected under 35 U.S.C. 102(b) as being anticipated by DeKoning et al. (US 6,178,520).

20. With respect to claim 11, DeKoning et al. disclose a method of installing a new memory that has a predetermined capacity and a new memory ID into a system that comprises

a processor (112 of Fig. 1) and  
first and second old memory (110 of Fig. 1)  
having respective first and second memory IDs (column 4, lines 23-27),  
first and second old memories, said memories capable of storing application data, comprising:

removing the first of old memory from the system (column 4, lines 6-10);  
installing the new memory into the system (column 4, lines 10-12);  
determining whether the new memory ID matches either of the first or second memory IDs (column 4, lines 23-27); and  
replicating the application data from the second old memory to the new memory if the new memory ID does not match either of the first or second memory IDs, to maintain a redundant array of independent memories (column 1, lines 43-45 describe how "the remaining available data and/or redundancy data is used to recreate the data missing due to the failure of a single disk drive").

***Claim Rejections - 35 USC § 103***

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krech, Jr. et al. (5,664,114) in view of McNutt et al. (US 5,659,705).

23. Claim 6 distinguishes over the teaching of Krech, Jr. et al. by the limitations of an application electrical connector on the application module; and a controller electrical connector on the electrical applications controller in communication with the application electrical connector; wherein each of said electrical connectors are axially symmetric to enable different relative rotational positions between the application and connector modules.

McNutt et al. disclose an application electrical connector on the application module ("Bus Expansion Port" or 32 on "Expansion Module" of Fig. 1); and a controller electrical connector on the electrical applications controller in communication with the application electrical connector (32 of Fig. 1); wherein each of said electrical connectors are axially symmetric to enable different relative rotational positions between the application and connector modules (Fig. 5).

It should be noted that the axis of symmetry is not specified in the drawings. The examiner has assumed the axis "running through the application module 165" (Detailed Description, page 11, lines 302-303) to be a line drawn perpendicularly to the face of the application module with connector 415 at its center, shown in Fig. 4. The connectors shown in Fig. 5 of McNutt et al. are clearly symmetric about an analogous axis, drawn perpendicularly to the face of 32 of Fig. 5 at its center.

Krech, Jr. et al. and McNutt et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention it would have been obvious to a person of ordinary skill in the art to apply the portability of the device of McNutt et al. to the architecture of Krech, Jr. et al. McNutt et al. teach the motivation for doing so as "a memory cartridge which may be reprogrammed in place by user command, then used to transport the user program and data to another PLC [Programmable Logic Controller, equivalent to processor]" (column 4, lines 61-63); this invention allow data to be stored on a removable memory cartridge and used on other processors. Therefore, it would have been obvious to combine Krech, Jr. et al. with McNutt et al. for the benefit of a portable data-transfer and storage device as specified in claim 6.

24. Claim 7 distinguishes over the teaching of Krech, Jr. et al. by the limitations of means for releasably connecting the application module to the electrical applications controller ("Bus Expansion Port" or 32 on "Expansion Module" of Fig. 1), said means enabling the application module and the electrical applications controller to be disengaged and break electrical communication between them (column 10, lines 29-30), rotated 180 degrees and reengaged to reestablish electrical communication between them (Fig. 5; column 6, lines 23-26 state that "it is to be understood that other connectors can and may be utilized without departing from the spirit and scope of the present invention," and this presumably includes connectors that allow the modules to be removed, rotated 180 degrees, and connected).

Krech, Jr. et al. and McNutt et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention it would have been obvious to a person of ordinary skill in the art to combine the portability of the device of McNutt et al. to the architecture of Krech et al. McNutt et al. teach the motivation for doing so is "a memory cartridge which may be reprogrammed in place by user command, then used to transport the user program and data to another PLC [Programmable Logic Controller, equivalent to processor]" (column 4, lines 61-63); this invention allow data to be stored on a removable memory cartridge and used on other processors. Therefore, it would have been obvious to combine Krech, Jr. et al. with McNutt et al. for the benefit of a portable data-transfer and storage device as specified in claim 7.

25. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over DeKoning et al. (US 6,178,520) in view of Krech, Jr. et al (US 5,664,114).

26. Claim 12 distinguishes over the teaching of DeKoning et al. wherein said new memory transmits an empty data indication to said processor if said new memory does not store any data, and said transmission enables said data replication.

Krech, Jr. et al. disclose said new memory transmitting an empty data indication to said processor if said new memory does not store any data (column 5, lines 10-12).

DeKoning et al. and Krech, Jr. et al. are analogous art because they are from the same field of endeavor, namely the transfer of data between memories.

At the time of invention, it would have been obvious to a person of ordinary skill in the art to apply the empty data indication of Krech, Jr. et al. to the drive detector system of DeKoning et al. The motivation for doing so would have been to avoid overwriting critical data, which is implied by Baentsch et al. because "the payload area

[of an already allocated block] contains application data that is critical to the application” (column 2, lines 58-59). Therefore, it would have been obvious to combine DeKoning et al. with Baentsch et al. for the benefit of a hot-swap detection system that automatically detected a new disk drive, verified that it had no application data already on it and replicated data onto it to obtain the invention as specified in claim 12.

***Relevant Art Cited by the Examiner***

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references teach a data storage system of similar design:

US 6,766,429, figure 3;

US 2003/0221077, figures 4 and 6;

US 6,587,909, figure 8;

US 6,892,276, figures 1-4, 6-7;

US 6,295,591, figure 2.

***Status of Claims in the Application***

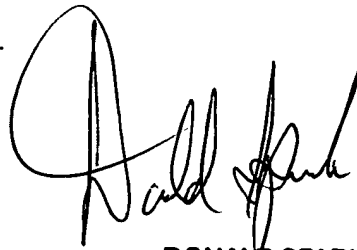
Claims rejected in the application: 1-12. Per the instant office action, claims 1-12 have received a first action on the merits and are subject of a first action non-final.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Golden, whose telephone number is 571-272-5628. The examiner can normally be reached on Monday-Friday, 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached at 571-272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to read 'Donald Sparks', is positioned above the printed name and title.

**DONALD SPARKS**  
**SUPERVISORY PATENT EXAMINER**